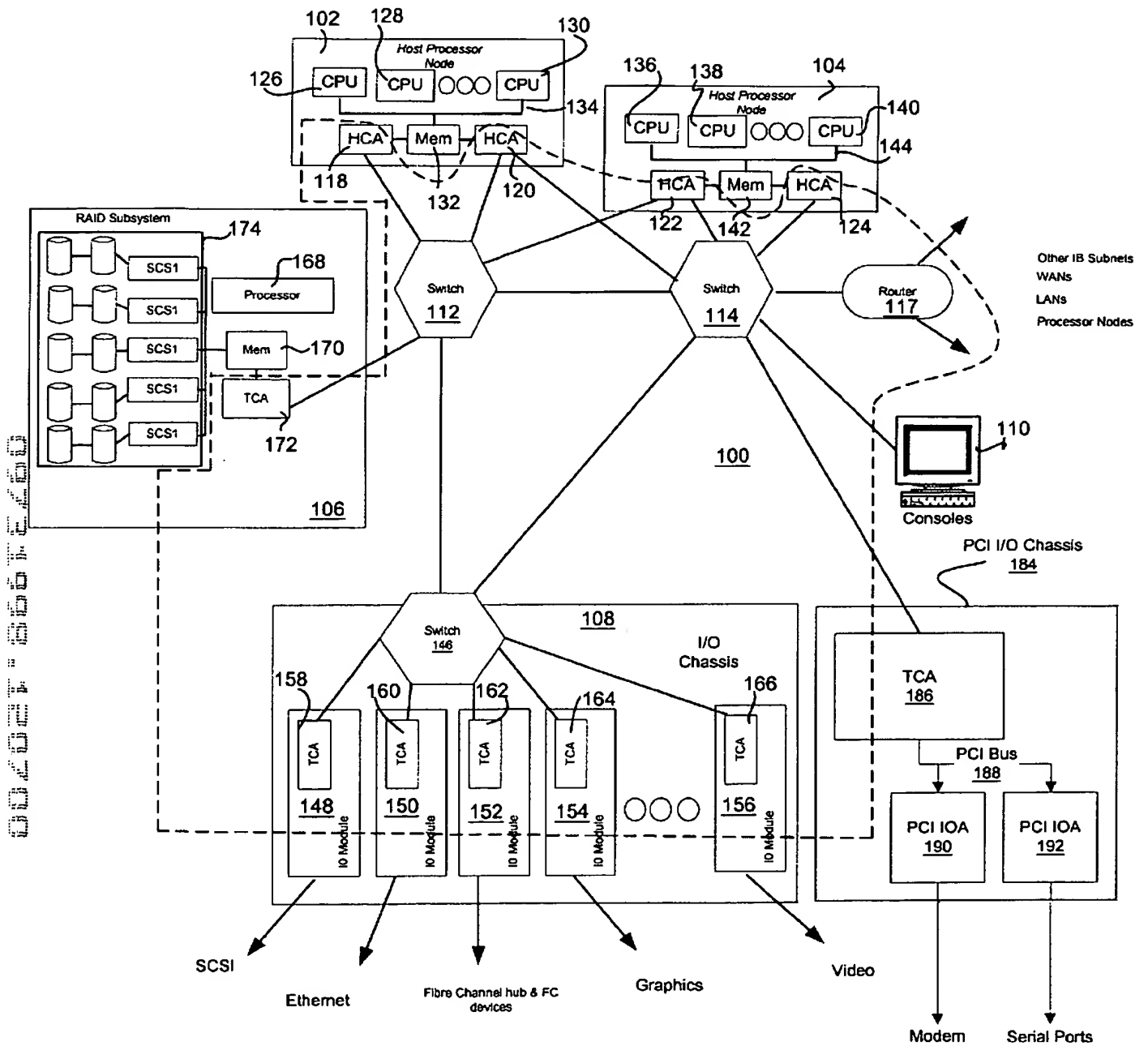


Figure 1

AUS9-2000-0546-US1



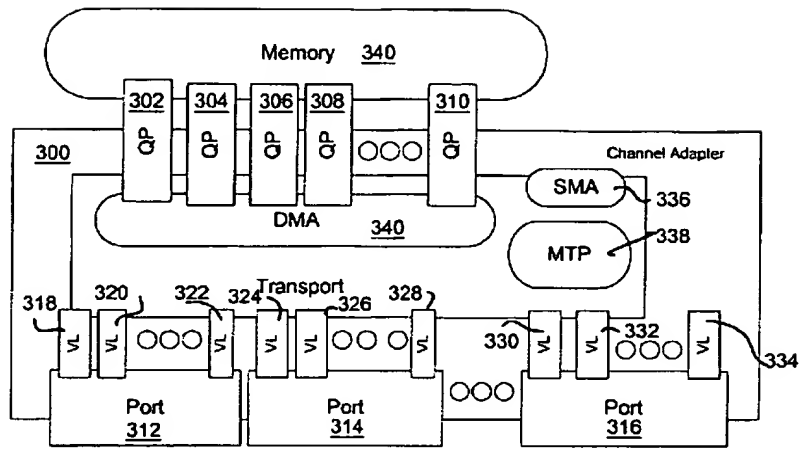


Figure 3

AUS9-2000-0546-US1

Figure 4

AUS9-2000-0546-US1

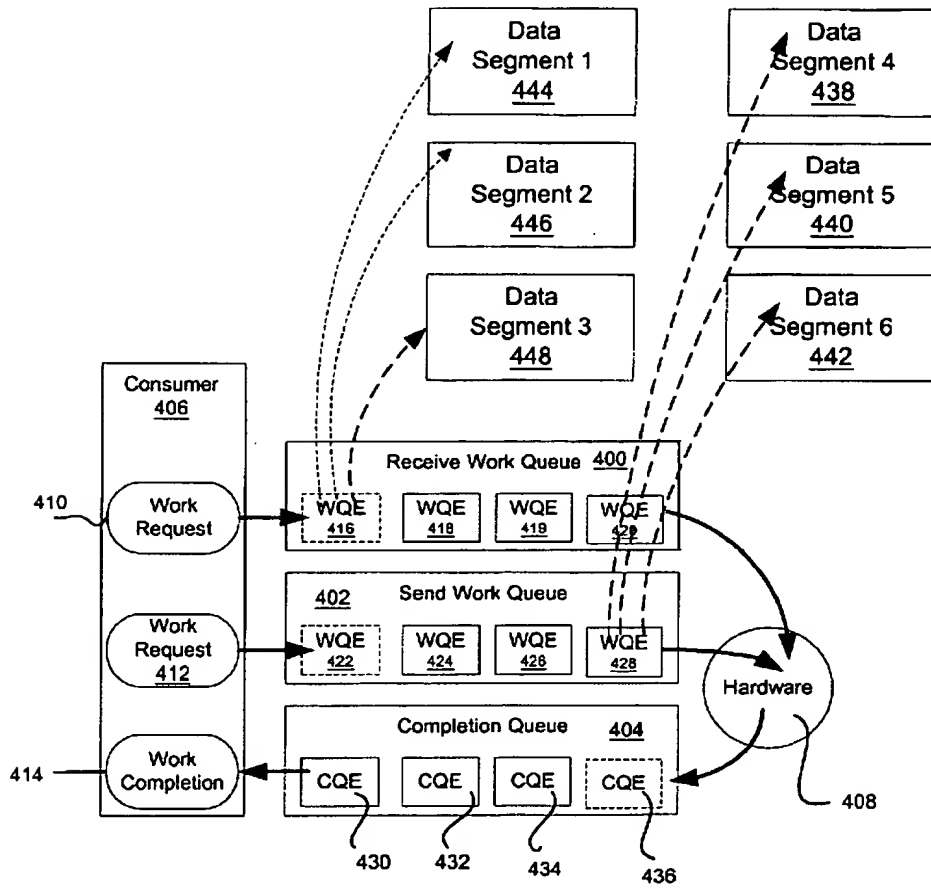


Figure 5

AUS9-2000-0546-US1

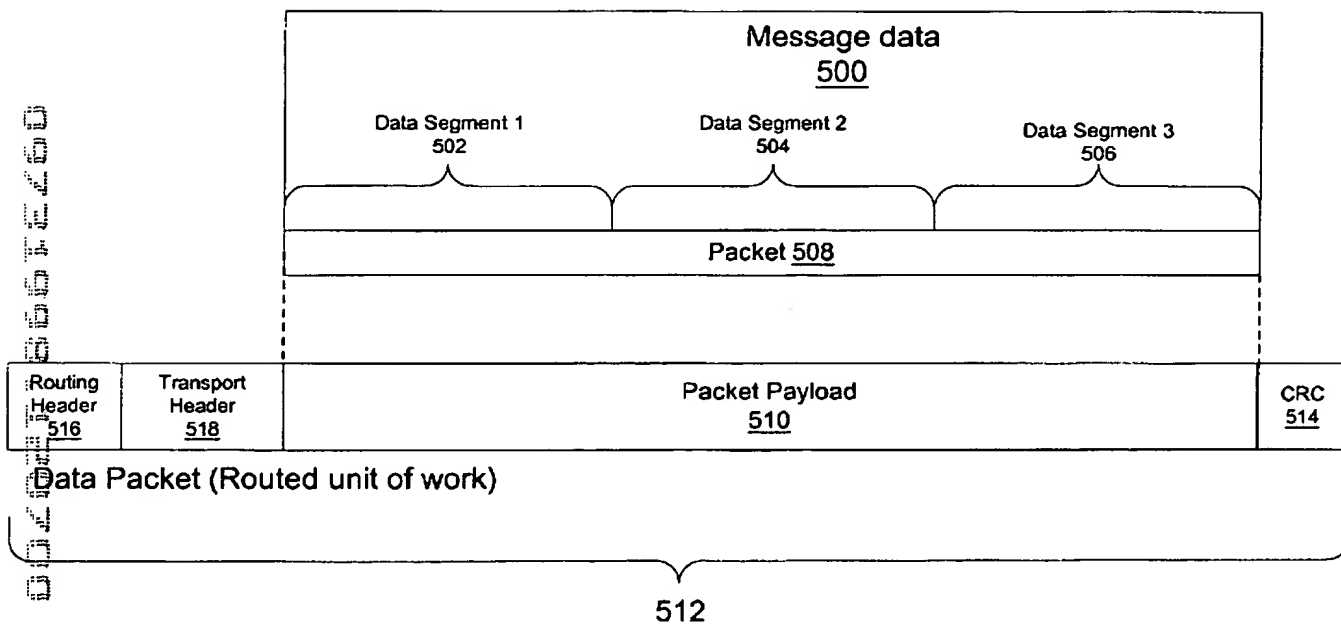


Figure 6

AUS9-2000-0546-US1

600

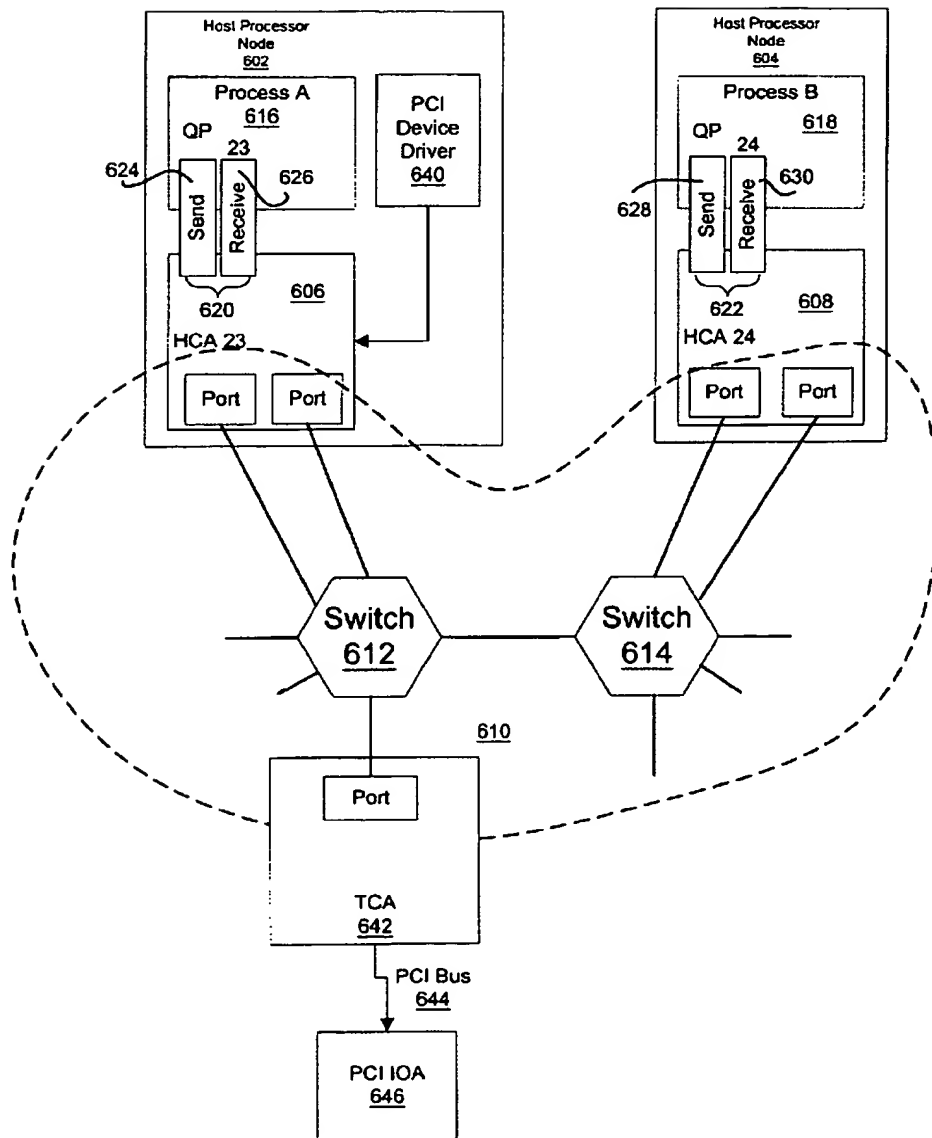
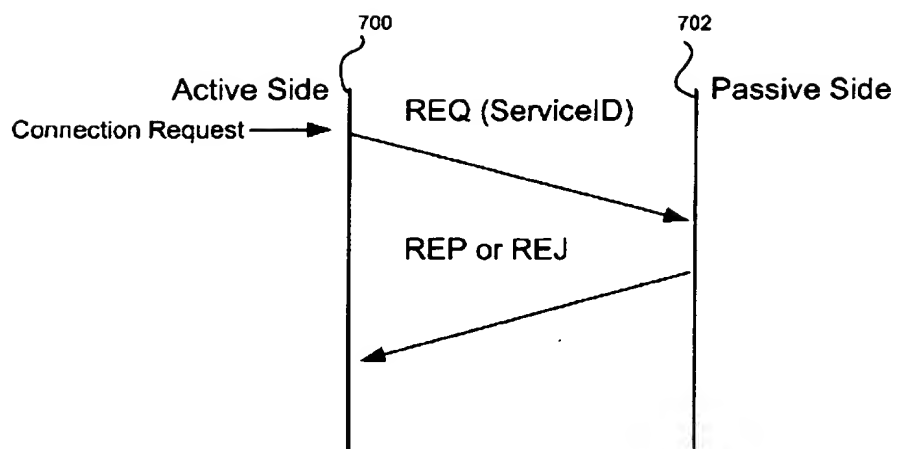


Figure 7

AUS9-2000-0546-US1



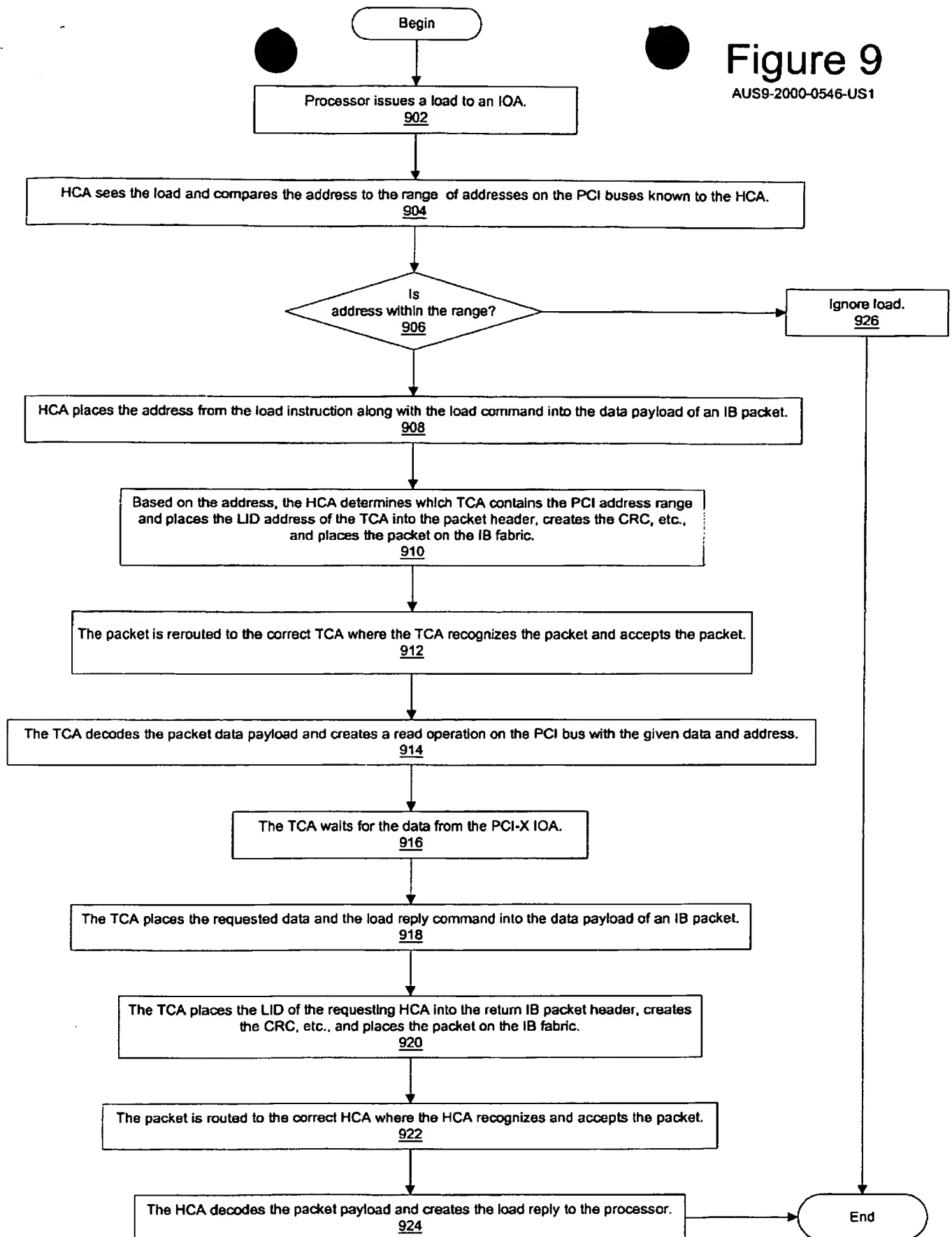
```

graph TD
    Start([Begin]) --> 802[Processor issues a store to an IOA.  
802]
    802 --> 804[HCA sees the store and compares the address to the range of addresses on the  
PCI buses known to the HCA.  
804]
    804 --> 806{Is  
address in range?  
806}
    806 -- NO --> 818[Ignore the store operation.  
818]
    806 -- YES --> 808[HCA places the address and data from the store instruction along with the store  
command into the data payload of an IB packet.  
808]
    808 --> 810[Based on the address decoded, the HCA determines which TCA contains the  
PCI address range and puts the LID address of the TCA into the packet header,  
creates the CRC, etc., and places the packet on the IB fabric.  
810]
    810 --> 812[Route the packet to the correct TCA.  
812]
    812 --> 814[The TCA recognizes and accepts the packet.  
814]
    814 --> 816[The TCA decodes the packet payload and creates a write operation on the PCI  
bus with the given data and address.  
816]
    816 --> End([End])
    818 --> End
  
```

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Figure 9

AUS9-2000-0546-US1



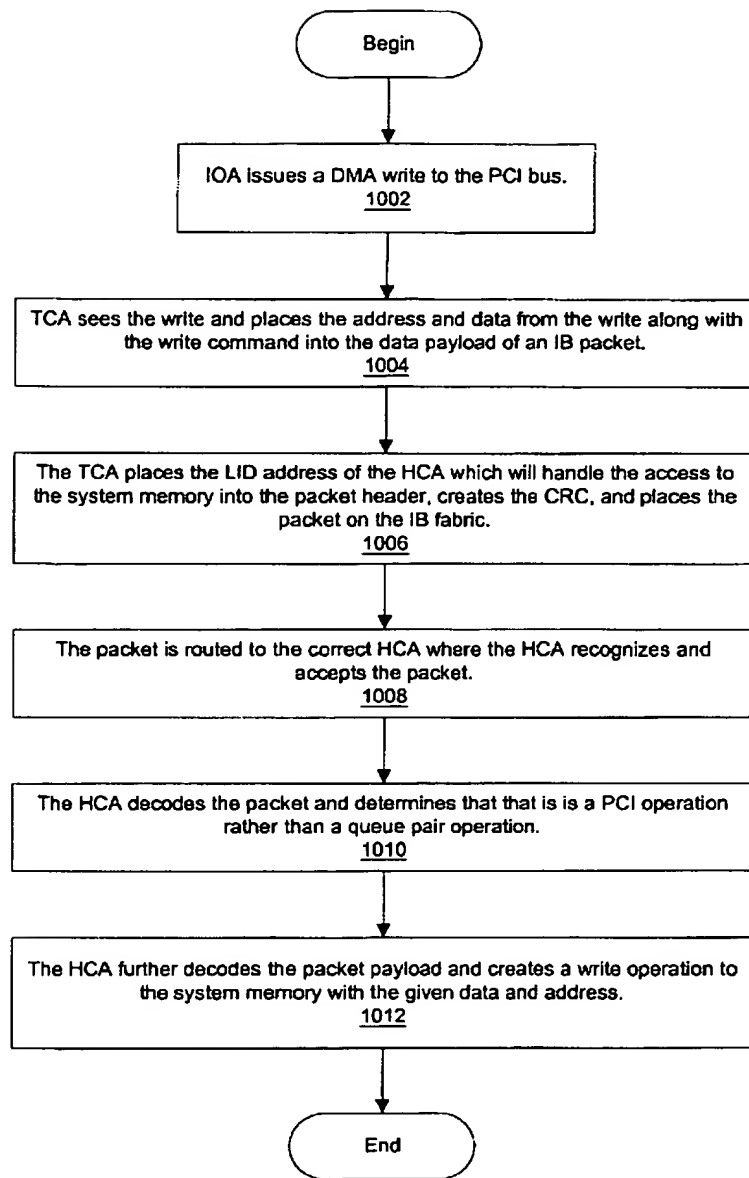


Figure 10
AUS9-2000-0546-US1

Figure 11
AUS9-2000-0546-US1

